GOVERNMENT COLLEGE OF TECHNOLOGY
(An Autonomous Institution Affiliated to Anna University)
Coimbatore - 641 013

Regulations, Curriculum And Syllabi For
M.E. (VLSI DESIGN )
(Full Time / Part Time)

2012 Regulations

OFFICE OF THE CONTROLLER OF EXAMINATIONS,
GOVERNMENT COLLEGE OF TECHNOLOGY
THADAGAM ROAD, COIMBATORE - 641 013

PHONE 0422 - 2433355  FAX : +91 0422 - 2433355
email : gctcoe@gmail.com
Curriculum
# CURRICULUM FOR CANDIDATES ADMITTED
DURING 2012-2013 AND ONWARDS
BRANCH: M.E. (VLSI DESIGN) - (FULL TIME)

## FIRST SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>THEORY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>12VL01</td>
<td>APPLIED MATHEMATICS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 1 0 4</td>
</tr>
<tr>
<td>2</td>
<td>12VL02</td>
<td>ADVANCED DIGITAL SYSTEM DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 1 0 4</td>
</tr>
<tr>
<td>3</td>
<td>12VL03</td>
<td>DIGITAL CMOS VLSI DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL04</td>
<td>COMPUTER AIDED VLSI DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>ELECTIVE I</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>ELECTIVE II</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td>600</td>
<td>20</td>
</tr>
</tbody>
</table>

## SECOND SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>THEORY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>12VL05</td>
<td>ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td>12VL06</td>
<td>LOW POWER VLSI DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td>12VL07</td>
<td>VLSI SIGNAL PROCESSING</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL08</td>
<td>ANALOG VLSI DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>ELECTIVE III</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>ELECTIVE IV</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td>600</td>
<td>18</td>
</tr>
</tbody>
</table>
### THIRD SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>12VL09</td>
<td>TESTING OF VLSI CIRCUITS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>ELECTIVE V</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>ELECTIVE VI</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL10</td>
<td>PROJECT -I</td>
<td>50</td>
<td>150</td>
<td>200</td>
<td>0 0 12 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td><strong>500</strong></td>
<td><strong>15</strong></td>
</tr>
</tbody>
</table>

### FOURTH SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL11</td>
<td>PROJECT -II</td>
<td>100</td>
<td>300</td>
<td>400</td>
<td>0 0 24 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td><strong>400</strong></td>
<td><strong>12</strong></td>
</tr>
</tbody>
</table>
# Curriculum for Candidates Admitted During 2012-2013 and Onwards

## Branch: M.E. (VLSI Design) - Part Time

### First Semester

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course Title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL01</td>
<td>Applied Mathematics</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 1 0 4</td>
</tr>
<tr>
<td>2</td>
<td>12VL02</td>
<td>Advanced Digital System Design</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 1 0 4</td>
</tr>
<tr>
<td>3</td>
<td>12VL03</td>
<td>Digital CMOS VLSI Design</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td>11</td>
</tr>
</tbody>
</table>

### Second Semester

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course Title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>12VL05</td>
<td>Analysis and Design of Analog Integrated Circuits</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td>12VL06</td>
<td>Low Power VLSI Design</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>12VL07</td>
<td>VLSI Signal Processing</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td>9</td>
</tr>
</tbody>
</table>

### Third Semester

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course Title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL04</td>
<td>Computer Aided VLSI Design</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Elective I</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Elective II</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td>9</td>
</tr>
</tbody>
</table>
### FOURTH SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Sessional marks</td>
<td>Final Exam marks</td>
<td>Total marks</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L T P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C</td>
</tr>
<tr>
<td>4</td>
<td>12VL08</td>
<td>ANALOG VLSI DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>ELECTIVE III</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>ELECTIVE IV</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td>300</td>
<td>9</td>
</tr>
</tbody>
</table>

### FIFTH SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Sessional marks</td>
<td>Final Exam marks</td>
<td>Total marks</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L T P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>12VL09</td>
<td>TESTING OF VLSI CIRCUITS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>ELECTIVE V</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>ELECTIVE VI</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL10</td>
<td>PROJECT - I</td>
<td>50</td>
<td>150</td>
<td>200</td>
<td>0 0 12 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td>500</td>
<td>15</td>
</tr>
</tbody>
</table>

### SIXTH SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Sessional marks</td>
<td>Final Exam marks</td>
<td>Total marks</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Sessional marks</td>
<td>Final Exam marks</td>
<td>Total marks</td>
<td>L T P C</td>
</tr>
<tr>
<td>1</td>
<td>12VL11</td>
<td>PROJECT - II</td>
<td>100</td>
<td>300</td>
<td>400</td>
<td>0 0 24 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOTAL</td>
<td></td>
<td></td>
<td>400</td>
<td>12</td>
</tr>
</tbody>
</table>
## ELECTIVES FOR M.E (VLSI DESIGN)

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL12</td>
<td>ADVANCED MICROPROCESSORS AND MICROCONTROLLERS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td>12VL13</td>
<td>NEURAL NETWORKS AND ITS APPLICATIONS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td>12VL14</td>
<td>ROBOTICS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL15</td>
<td>ADVANCED DIGITAL SIGNAL PROCESSING</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td>12VL16</td>
<td>SOLID STATE DEVICES MODELLING AND SIMULATION</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>12VL17</td>
<td>SYSTEM DESIGN LABORATORY</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>0 0 4 3</td>
</tr>
</tbody>
</table>

### ELECTIVE III, IV

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL18</td>
<td>MIXED SIGNAL CIRCUIT DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td>12VL19</td>
<td>DSP INTEGRATED CIRCUITS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td>12VL20</td>
<td>ASIC DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL21</td>
<td>ADVANCED EMBEDDED SYSTEMS</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td>12VL22</td>
<td>BIO-SIGNAL PROCESSING</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>12VL23</td>
<td>ADVANCED VLSI DESIGN LABORATORY</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>0 0 4 3</td>
</tr>
</tbody>
</table>

### ELECTIVE V, VI

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Subject Code</th>
<th>Course title</th>
<th>Sessional marks</th>
<th>Final Exam marks</th>
<th>Total marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12VL24</td>
<td>MOBILE COMMUNICATION</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>2</td>
<td>12VL25</td>
<td>EMBEDDED NETWORKING</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>3</td>
<td>12VL26</td>
<td>SYSTEM ON CHIP</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>4</td>
<td>12VL27</td>
<td>RELIABILITY ENGINEERING</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>5</td>
<td>12VL28</td>
<td>VLSI FOR WIRELESS COMMUNICATION</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
<tr>
<td>6</td>
<td>12VL29</td>
<td>INTRODUCTION TO MEMS SYSTEM DESIGN</td>
<td>25</td>
<td>75</td>
<td>100</td>
<td>3 0 0 3</td>
</tr>
</tbody>
</table>
LINEAR INTEGRAL EQUATIONS

SPECIAL FUNCTION
Bessel’s equation – Bessel’s functions – Legendre’s equation – Polynomials – Rodrigue’s Formula – Recurrence Relations – Generating Functions – Orthogonal Property for Bessel’s function of first kind.

CALCULUS OF VARIATION
Functional – Euler’s Equation – Variational Problems involving one unknown Function, Several unknown functions – Functional dependent on higher order derivatives – Several independent variables – Isoperimetric problems.

RANDOM PROCESSES

QUEUING THEORY
Characteristic and representation of Queuing Models – Model I : [(M/M/1) : (“/FIFO) , Model II : [(M/M/S) : (“/FIFO) Model III : [(M/M/1) : (N/FIFO)], Model IV : [(M/M/S) : (N/FIFO)]

LECTURE:45 TUTORIAL:15 TOTAL:60 HOURS

Reference books
12VL.02 ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. Applied Electronics)

LOGIC DESIGN WITH VERILOG HDL
Primitives - Keywords - Data types - Operators - Formal syntax - additional features of Verilog - Programming language interface - Fundamentals of combinational and sequential logic designs - logic design of behavioral structural and data flow models of combinational and sequential logics.

SEQUENTAIL CIRCUIT DESIGN
Analysis of Clocked Synchronous Sequential Networks (CSSN), Modeling of CSSN - state stable assignment and reduction - Design of CSSN - Design of Iterative circuits - ASM Chart - ASM Realization - Sequential logic design and synthesis with Latches, Flip-flops, Registers and Counters.

SYNCHRONOUS DESIGN USING PROGRAMMABLE LOGIC DEVICES

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Races in ASC - State Assignment - Problems and the Transition Table - Design of ASC - State and Dynamic Hazards - Essential Hazards - Data Synchronizers - Designing Vending Machine Controllers - Mixed Operating Mode Asynchronous Circuits - Introduction to logic design and synthesis of RISC stored program machine - Binary counters and UART.

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

LECTURE: 45 TUTORIAL: 15 TOTAL: 60 HOURS

Reference books
12VL03 DIGITAL CMOS VLSI DESIGN  
(Common to M.E. Applied Electronics)

MOS INVERTER AND LOGIC GATES
MOS Inverter and its characteristics: Introduction- Inverter- Static CMOS inverter- Propagation delay of inverter- CMOS inverter power dissipation. Logic Gates: Introduction- Combinational logic functions- Static Complementary gates- Switch logic- Alternative gate circuits- Low power gates- Delay through resistive and inductive interconnect

COMBINATIONAL STATIC LOGIC NETWORKS
Introduction- MOS logic- Complementary logic- AOI and OAI gates- Pseudo-nMOS Logic- Differential voltage logic styles- PTL- Complementary and Double PTL- Standard cell-based layout- Combinational network delay- Power optimization- Combinational logic testing.

SEQUENTIAL LOGIC CIRCUITS
Introduction- Sequential logic circuit- Latch- Flip-flop - Registers and counters- Sequential systems and clocking disciplines- Clock generation- Sequential system design- Power optimization.

SEMICONDUCTOR MEMORY AND ARITHMETIC CIRCUITS
Introduction- RAM- SRAM- Non-volatile memory. Adder and Multiplier circuits- Adder circuits- CMOS adder architecture- Subtractor- Multiplier- ALU.

ARCHITECTURE DESIGN
Introduction- Hardware Description Languages- Register –Transfer Design- Pipelining- High-level synthesis- Design methodologies- Multiprocessor System-on-chip design.

TOTAL : 45 HOURS

Reference books
12VL04 COMPUTER AIDED VLSI DESIGN

INTRODUCTION TO VLSI DESIGN METHODOLOGIES
VLSI Design Cycle - Physical Design Cycle - Design Styles and comparison of different Design Styles - Fabrication of VLSI Circuits.

VLSI DESIGN AUTOMATION

PHYSICAL DESIGN

SIMULATION AND SYNTHESIS
Simulation - Gate Level Modelling and Simulation - Switch Level Modelling and Simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis

HIGH LEVEL SYNTHESIS
Hardware Models - Internal Representation - Allocation assignment and scheduling - Simple Scheduling Algorithm - Assignment Problem.

TOTAL: 45 HOURS

Reference books
MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES
Depletion Region of a pn junction - Small signal model of a bipolar transistor - Large Signal behavior of bipolar transistors - Large Signal Behaviour of MOSFET - Small signal model of the MOS transistors.

CIRCUIT CONFIGURATION FOR LINEAR IC

NON LINEAR ANALOG CIRCUITS
Precision Rectification - Analysis of four quadrant and variable transconductance multiplier - Application of Gilbert cell. Balanced Modulator - Closed loop analysis of PLL - Voltage Controlled Oscillator.

OPERATIONAL AMPLIFIER
Analysis of operational amplifier circuit, Slew rate model and High Frequency Analysis - Operational Amplifier noise.

ANALOG DESIGN WITH MOS TECHNOLOGY

TOTAL : 45 HOURS

Reference books
12VL06 LOW POWER VLSI DESIGN
(Common to M.E. Applied Electronics)

DEVICE & TECHNOLOGY IMPACT ON LOW POWER
Need for low power VLSI chips - Sources of power dissipation on Digital Integrated circuits - Emerging Low power approaches - Physics of power dissipation in CMOS devices - Dynamic dissipation in CMOS - Transistor sizing & Gate oxide thickness - Impact of technology Scaling - Technology and Device innovation.

SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS
SPICE circuit simulators - Gate level logic simulation - Capacitive power estimation - Static state power - Gate level capacitance estimation - Architecture level analysis - Monte Carlo simulation - Random logic signals - probability and frequency - probabilistic power analysis techniques - signal entropy.

LOW POWER DESIGN
Circuit level: Power consumption in circuits - Flip Flops and Latches design - High capacitance nodes - Low power digital cells library - Logic level: Gate reorganization - signal gating - logic encoding - state machine encoding - pre computation logic.

LOW POWER ARCHITECTURES AND CLOCK DISTRIBUTION
Power & Performance management - switching activity reduction - Parallel architecture with voltage reduction - Flow graph transformation - Low power arithmetic components - Low power memory design - Power dissipation in clock distribution - Single driver vs Distributed buffers - Zero skew vs tolerable skew - Chip and package co-design of clock network

ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES
Introduction - Design flow - Algorithmic level analysis and optimization - Architectural level estimation and synthesis.

TOTAL : 45 HOURS

Reference books
12VL07 VLSI SIGNAL PROCESSING
(Common to M.E. Applied Electronics)

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ITERATION BOUND

UNFOLDING

FAST CONVOLUTION

BITLEVEL ARITHMETIC ARCHITECTURES

NUMERICAL STRENGTH REDUCTION

TOTAL: 45 HOURS

Reference books
12VL08 ANALOG VLSI DESIGN
(Common to M.E. Applied Electronics)

BASIC CMOS CIRCUIT TECHNIQUE
Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage- Super MOS Transistor- Primitive Analog Cells-
Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS - Bipolar and Low-Voltage BiCMOS Op-
Amp Design-Instrumentation Amplifier Design.

NEURAL INFORMATION PROCESSING
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Inspired Neural
Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-
Contrast Sensitive Silicon Retina.

SAMPLED DATA ANALOG FILTERS
First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis
of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second
Order and Multibit Sigma-Delta Modulators-Interpolative Modulators.

DESIGN FOR TESTABILITY
Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-
Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testability-Physics of Interconnects in
VLSI-Scaling of Interconnects.

STATISTICAL MODELING AND SIMULATION
Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed
Analog -Digital Layout.

TOTAL:45 HOURS

Reference books
Processing “, Prentice Hall, 1994
12VL09 TESTING OF VLSI CIRCUITS
(Common to M.E. Applied Electronics)

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BASICS OF TESTING AND FAULT MODELING

TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS
Test generation for Combinational logic circuits - Testable Combinational logic circuit design - Test generation for Sequential circuits - Design of Testable sequential circuits.

DESIGN FOR TESTABILITY
Design for Testability - Ad-hoc design - Generic Scan based design - Classical scan based design - System level DFT approaches.

SELF-TEST AND TEST ALGORITHMS
Built-in self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test Algorithms - Test generation for Embedded RAMs.

FAULT DIAGNOSIS
Logical Level Diagnosis - Diagnosis by Unit Under Test reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System level Diagnosis.

TOTAL: 45 HOURS

Reference books
12VL12 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

(Common to M.E. Applied Electronics)

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MICROPROCESSOR ARCHITECTURE

Instruction set-Data formats -Instruction formats -Addressing Modes-Memory hierarchy- register file-Cache-Virtual memory and paging-Segmentation-Pipelining-Instruction pipeline-pipeline hazards-Instruction level parallelism-Reduced instruction set-Computer principles-RISC versus CISC-RISC properties-RISC evaluation-On-chip register files versus cache evaluation.

HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM^ (9)


HIGH PERFORMANCE RISC ARCHITECTURE: ARM (9)

The ARM architecture-ARM Assembly Language Program-ARM Organization and Implementation-The ARM instruction set-The Thumb instruction set-ARM CPU cores.

MOTOROLA 68HC11 MICROCONTROLLERS (9)

Instructions and addressing modes-operating modes-Hardware reset-Interrupt system- Parallel I/O ports-Flags-Real time clock-Programmable timer-pulse accumulator-serial communication interface-A/D converter-hardware expansion-Assembly language Programming.

PIC MICRO CONTROLLER (9)

CPU architecture-Instruction set-Interrupts-Timers-I/O port expansion-I2C bus for peripheral chip access-A/D converter-UART.

TOTAL: 45 HOURS

Reference books

12VL13 NEURAL NETWORKS AND ITS APPLICATIONS
(Common to M.E. Applied Electronics)

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INTRODUCTION
Artificial neural networks - History-Structure and function of single neuron-Weights, activation functions and bias-
Fundamental neuron models and learning-Neural net architectures-Learning algorithms, supervised and unsupervised-
Use of neural networks - Perceptron- linear separability.

FEED FORWARD AND FEEDBACK NETWORKS

SIMULATED ANNEALING AND COMPETITIVE NETWORKS
Annealing-Boltzman machine architecture, learning and processing-Practical considerations-Neural networks based on competition-Counter propagation network-Forward mapping CPN and complete CPN-Building blocks-Architecture, Training and data processing-Practical considerations and applications.

SOM AND ADAPTIVE RESONANCE THEORY

HANDWRITTEN CHARACTER AND SPEECH RECOGNITION

TOTAL:45 HOURS

Reference books
12VL14 ROBOTICS
(Common to M.E. Applied Electronics)

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INTRODUCTION TO ROBOTICS

COMPUTER VISION

SENSORS AND SENSING DEVICES

ARTIFICIAL INTELLIGENCE

INTEGRATION TO ROBOT
Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - Algorithms for path finding and decision making

TOTAL: 45 PERIODS

Reference books
12VL15 ADVANCED DIGITAL SIGNAL PROCESSING  
(Common to M.E. Applied Electronics)

**DISCRETE RANDOM SIGNAL PROCESSING**


**SPECTRAL ESTIMATION**


**LINEAR ESTIMATION AND PREDICTION**

Linear prediction – Forward and Backward prediction- Solution of Prony’s normal equations- Least mean-squared error criterion- Wiener filter for filtering and prediction- FIR and IIR Wiener filters- Discrete Kalman filter.

**ADAPTIVE FILTERS**


**MULTIRATE DIGITAL SIGNAL PROCESSING**

Mathematical description of change of sampling rate – Interpolation and Decimation- Decimation by an integer factor- Interpolation by an integer factor- Sampling rate conversion by a rational factor- Polyphase filter structures - Time invariant structures - Multistage implementation of multirate system- Application to subband coding – Wavelet transform.

**TOTAL: 45 HOURS**

**Reference books**


12VL16 SOLID STATE DEVICES MODELLING AND SIMULATION

BASIC SEMICONDUCTOR PHYSICS


MODELING BIPOLAR DEVICE PHENOMENA

Injection and Transport Model- Continuity Equation- Diode Small Signal and Large Signal (Change Control Model)- Transistor Models: Ebber - Molls and Gummel Port Model- Mextram model- SPICE modeling temperature and area effects.

MOSFET MODELING

Introduction Interior Layer- MOS Transistor Current- Threshold Voltage- Temperature Short Channel and Narrow Width Effect- Models for Enhancement- Depletion Type MOSFET- CMOS Models in SPICE.

PARAMETER MEASUREMENT


OPTOELECTRONIC DEVICE MODELS

Static and Dynamic Models- Rate Equations- Numerical Technique- Equivalent Circuits- Modeling of LEDs- Laser Diode and Photo Detectors

TOTAL : 45 HOURS

Reference books

12VL17 SYSTEM DESIGN LABORATORY

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I. Implementation of Embedded System Design using Proteus, Keil, Microcontroller 8051 trainer kit
   ● Real-time clock
   ● Frequency Generation and Serial Communication
   ● Manual Timer Set
   ● Automatic Car Parking using Counter

II. Implementation of Embedded System Design using MPLAB, HITECH C, PIC controller kit
   ● Home Control using GSM Interface
   ● External Memory Interface using FC bus
   ● CD Interface

III. Digital Design Modeling using HDL
   ● Verilog
   ● VHDL

IV. Implementation of VLSI system design using SPARTAN 3E FPGA
   ● LCD interface
   ● Keypad interface

V. Experiments using Xilinx EDK Tool

TOTAL: 45 HOURS

Reference books
4. Lab manuals
12VL18 MIXED SIGNAL CIRCUIT DESIGN

SINGLE STAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIERS (9)

CURRENT MIRRORS AND NOISE CHARACTERISTICS (9)

OPERATIONAL AMPLIFIERS (9)

NON LINEARITY AND SWITCHED CAPACITOR CIRCUITS (9)

PLLs AND DATA CONVERTORS (9)
Simple PLL - Charge-pump PLLs - Non ideal effects in PLLs: PFD/CP non idealities - jitter in PLLs - Delay-locked loops - PLL applications - Analog versus discrete time signals - Sample and hold characteristics - ADC and DAC specifications - DAC architectures - ADC architectures - Sampling and aliasing - Quantization noise & Data converter SNR - CCD imaging and architecture.

TOTAL: 45 HOURS

Reference books
12VL19 DSP INTEGRATED CIRCUITS

(Common to M.E. Applied Electronics)  

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DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES (9)
Standard digital signal processors - Application specific IC’s for DSP - DSP systems - DSP system design - Integrated circuit design - MOS transistors - MOS logic - VLSI process technologies

DIGITAL SIGNAL PROCESSING (9)

DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS (9)

DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES (9)
DSP system architectures - Ideal DSP architectures – Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit - serial PEs.

NUMBER SYSTEMS - ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN (9)
Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size – Complex multipliers - Layout of VLSI circuits

TOTAL:45 HOURS

Reference books
12VL20 ASIC DESIGN
(Common to M.E. Applied Electronics)

FUNDAMENTALS OF ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN (9)
Types of ASICs-Design flow-CMOS Transistors CMOS Design Rules -Combinational Logic Cell-Sequential Logic cell-
Data path Logic Cell-Transistors as Resistors-Transistor Parasitic Capacitance-Logical effort-Library Cell Design-Library
Architecture.

PROGRAMMABLE ASICS (9)
Anti fuse-Static RAM-EPROM and EEPROM technology-PREP benchmarks-Actel ACT-Xilinx LCA-Altera FLEX-
Altera MAX DC and AC inputs and outputs-Clock and Power inputs-Xilinx I/O blocks.

PROGRAMMABLE ASIC INTERCONNECT, DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY (9)
Actel ACT-Xilinx LCA-Xilinx EPLD-Altera MAX 5000 and 7000-Altera MAX 9000-Altera FLEX-Design Systems-
Logic Synthesis-Half gate ASIC-Schematic entry-Low level design language-PLA tools-EDIF-CFI design representation

LOGIC SYNTHESIS - SIMULATION AND TESTING (9)
Verilog and Logic Synthesis -VHDL and Logic Synthesis - Types of Simulation -Boundary Scan Test - Fault simulation-
Automatic Test Pattern Generation.

ASIC CONSTRUCTION (9)
System partition-FPGA partitioning-Partitioning methods-Floor planning-placement-Physical Design Flow-Global Routing-
Detailed Routing-Special Routing-Circuit extraction- DRC.

TOTAL : 45 HOURS

Reference books
2. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs – A Practical Approach”, Prentice Hall
12VL21 ADVANCED EMBEDDED SYSTEMS
(Common to M.E. Applied Electronics)

INTRODUCTION AND REVIEW OF EMBEDDED HARDWARE
Terminology - Gates - Timing diagram - Memory - Microprocessor buses - Direct memory access - Interrupts - Built
interrupts - Interrupts basis - Shared data problems - Interrupt latency - Embedded system evolution trends - Round robin
- Round robin with interrupt function - Rescheduling architecture - algorithm.

REAL TIME OPERATING SYSTEM
Task and Task states - Task and data - Semaphore and shared data operating system services - Message queues timing
functions - Events - Memory management - Interrupt routines in an RTOS environment - Basic design using RTOS.

EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS
Custom single purpose processors: Hardware - Combination Sequence - Processor design - RT level design - optimising
software: Basic Architecture - Operation - Programmers view - Development Environment - ASIP - Processor Design
- Peripherals - Timers, counters and watch dog timers - UART - Pulse width modulator - LCD controllers - Key pad
controllers - Stepper motor controllers - A/D converters - Real time clock.

MEMORY AND INTERFACING
Memory: Memory write ability and storage performance - Memory types - composing memory Advance RAM interfacing
communication basic - Microprocessor interfacing I/O addressing Interrupts - Direct memory access - Arbitration
multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example.

CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO - DESIGN
Modes of operation - Finite state machines - Models - HCFSL and state charts language - state machine models -
Concurrent process model - Concurrent process - Communication among process - Synchronization among process -
Implementation - Data Flow model. Design technology - Automation synthesis - Hardware software co - simulation - IP
cores - Design Process Model.

TOTAL : 45 HOURS

Reference books
12VL22 BIO-SIGNAL PROCESSING
(Common to M.E. Applied Electronics)

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SIGNALS AND SYSTEMS

TIME SERIES ANALYSIS AND SPECTRAL ESTIMATION
Time series analysis-Linear prediction models, process order estimation, lattice representation, Non stationary process, Fixed segmentation, Adaptive segmentation, Application in EEG,PCG signals,Time varying analysis of Heart rate variability-model based ECG simulator, Spectral Estimation-Blackman Turkey method, periodogram and model based estimation, Applications in Heart-rate variability and PCG Signals.

ADAPTIVE FILTERING AND WAVELET DETECTION

BIOSIGNAL CLASSIFICATION AND RECOGNITION

TIME FREQUENCY AND MULTIVARIATE ANALYSIS
Time frequency representation-Spectrogram -Wigner distribution-Time Scale representation-Scalogram, Wavelet analysis-Data reduction techniques, ECG data compression-ECG characterization,Feature extraction-Wavelet packets, Multivariate component analysis-PCA,ICA.

TOTAL:45 HOURS

Reference books
PART I: Backend VLSI Design

I. SPICE simulation of NMOS and CMOS models
   - Inverter
   - Common source amplifier

II. Experiments using CADENCE/Synopsis
   - RTL realization
   - Boolean optimization
   - Static Timing Analysis
   - Layout Generation for Circuit Modules
   - LVS, Back annotation

III. Mixed mode signal design using CADENCE

PART II

I. Experiments using MATLAB Toolboxes

II. Image and Video processing experiments using Xilinx System Generator.

III. Implementation of Edge detection using various filters by SPARTAN 6 and VIRTEX 5 FPGA

TOTAL: 45 HOURS

Reference books


3. Lab manuals.
12VL24 MOBILE COMMUNICATION

(Common to M.E. Applied Electronics)

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CELLULAR CONCEPT AND SYSTEM DESIGN FUNDAMENTALS

(9)

Introduction to wireless communication- Evolution of mobile communications- mobile radio systems Examples- trends in cellular radio and personal communications- Cellular Concept- Frequency reuse- channel assignment- hand off- Interference and system capacity- tracking and grade of service- Improving Coverage and capacity in Cellular systems.

MOBILE RADIO PROPAGATION

(9)

Free space propagation model- reflection- diffraction- scattering- link budget design- Outdoor Propagation models- Indoor propagation models- Small scale Multipath propagation- Impulse model- Small scale Multipath measurements- parameters of Mobile multipath channels- types of small scale fading- statistical models for multipath fading channels.

MODULATION TECHNIQUES AND EQUALIZATION

(9)


CODING AND MULTIPLE ACCESS TECHNIQUES

(9)

Coding- Vocoders- Linear Predictive Coders- Selection of Speech Coders for Mobile Communication- GSM Codec- RS codes for CDPD- Multiple Access Techniques- FDMA- TDMA- CDMA- SDMA- Capacity of Cellular CDMA and SDMA.

WIRELESS SYSTEMS AND STANDARDS

(9)

Second Generation- Third Generation and Fourth Generation Wireless Networks and Standards- WLL- Blue tooth. AMPS- GSM- IS-95 and DECT

TOTAL: 45 HOURS

Reference books

12VL25 EMBEDDED NETWORKING
(Common to M.E. Applied Electronics)

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CAN OPEN INTRODUCTION
Embedded networking - code requirements - Communication requirements - Introduction to CAN open - CAN open standard - Configuration files - Network management CAN open messages - Device profile encoder - Evaluating system requirements choosing devices and tools Network simulation - Network Commissioning - Advanced features and testing.

CAN INTRODUCTION
Controller Area Network - Underlying Technology CAN Overview - Selecting a CAN Controller - CAN development tools.

CAN IMPLEMENTATION
Implementing CAN open Communication layout and requirements - Comparison of implementation methods - Micro CAN open - CAN open source code - Conformance test - Entire design life cycle.

SERIAL COMMUNICATION PROTOCOL
SPI - Data Transfer and signals, Modes, Microware. IIC - Data and Clock, Device addresses, Modes, single master and multiple master, arbitration, difference between SMBUS and I2C. MODBUS - Modes - TCP/IP, RTU, Message framing, Error Checking PCI-E - data transmission

PARALLEL COMMUNICATION PROTOCOL
Parallel P-ATA - PIO, DMA and ultra DMA modes, IDE, EIDE, ATAPI. PCI - bus - transaction of data and arbitration, PCI bridge.

TOTAL: 45 HOURS

References
4. www.modbus.org
5. www.pcisig.com
12VL26 SYSTEM ON CHIP
(Common to M.E. Applied Electronics)

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INTRODUCTION TO PROCESSOR DESIGN & ARM ARCHITECTURE

ARM ASSEMBLY LANGUAGE PROGRAMMING
ARM Instruction Types - Data Transfer, Data Processing and Control Flow Instructions - ARM Instruction Set - Co-processor Instructions.

ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGUAGE & MEMORY HIERARCHY
Abstraction in software design - Expressions - Loops - Functions and Procedures - Conditional Statements - Use of Memory. MEMORY HIERARCHY: Memory Size and Speed - On chip Memory - Caches - Cache Design - an Example - Memory Management.

ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT

ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM:
An Introduction to operating systems - ARM System Control Coprocessor - CP15 Protection Unit Registers – ARM Protection Unit - CP15 MMU Registers - ARM MMU Architecture - Synchronization - Context Switching Input and Output.

TOTAL: 45 HOURS

Reference books
12VL27 RELIABILITY ENGINEERING
(Common to M.E. Applied Electronics)

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PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE
(9)

RELIABILITY PREDICTION - MODELLING AND DESIGN
(9)
Statistical design of experiments and analysis of variance Taguchi method - Reliability prediction - Reliability modelling - Block diagram and Fault tree Analysis - Petric Nets - State space Analysis - Monte Carlo simulation - Design analysis methods - quality function deployment - load strength analysis - failure modes - effects and criticality analysis.

ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY
(9)
Reliability of electronic components - component types and failure mechanisms - Electronic system reliability prediction - Reliability in electronic system design - software errors - software structure and modularity - fault tolerance - software reliability - prediction and measurement - hardware/software interfaces.

RELIABILITY TESTING AND ANALYSIS
(9)
Test environments - testing for reliability and durability - failure reporting - Pareto analysis - Accelerated test data analysis - CUSUM charts - Exploratory data analysis and proportional hazards modelling - reliability demonstration - reliability growth monitoring.

MANUFACTURE AND RELIABILITY MANAGEMENT
(9)

TOTAL: 45 HOURS

Reference books
12VL28 VLSI FOR WIRELESS COMMUNICATION

ANALOG TO DIGITAL CONVERSION

CODING THEORY ALGORITHMS AND ARCHITECTURE

TRANSCIEVER ARCHITECTURE AND ISSUES
Receiver Architectures - Superheterodyne receiver - Image rejection receiver - Hartley and Weaver - Zero IF receiver - Low IF receiver - Transmitter architecture - Superheterodyne transmitter - Direct up transmitter - Two-step-up transmitter - Transceiver architectures for modern wireless systems - Case study.

OFDM SYSTEM
Principle - propagation characteristics - principle - mathematical model - OFDM baseband signal processing - Receiver design - Automatic gain control and DC offset compensation - codesign of Automatic gain control and timing synchronization - codesign of filtering and timing synchronization - Transmit chain setup.

ANALOG IMPAIRMENT AND ISSUES
Receiver sensitivity and noise figure - DC offsets - LO leakage - Receiver interferers and intermodulation distortion - Image rejection - Quadrature balance and relation to Image rejection - relation to EVM - Peak to average power ratio - Local oscillator pulling in PLL - effect of phase noise in PLL - Effect of phase noise on OFDM systems - Effect of frequency errors on OFDM systems.

TOTAL: 45 HOURS

Reference books